PROSAK IC – PROgrammable Stand Alone Knock

User's Guide

1. Engine Knock Signal Processing

The PROSAK IC features a knock detection system that can interface with two knock sensors. The knock circuit uses an A/D converter, a fully programmable digital IIR filter, and knock signal detection processing. The IIR filters can be programmed per application requirements, or the knock system can be tailored using the calibration data port. The IC is designed to function for engines from three cylinders to twelve cylinders.

The knock sensor input is processed during a gating window function (WINK, WINR) generated externally via a microprocessor or custom circuitry. The PROSAK IC can be run in a single-window per cylinder mode (knock window only) or a dual-window per cylinder mode (knock window plus reference window). The knock sensor signals are filtered and integrated during the window events, and the output of the integrators can then be read directly through the SPI interface for software evaluation. The PROSAK IC also includes on-chip processing of the knock sensor signals and is capable of determining a knock condition via thresholding of knock signal intensity. The IC triggers a digital output pin (KO) when knock is indicated.

1.1 Features:

- Two Sensor Inputs
- Fully programmable 8th order digital IIR filter
- On-chip integration of knock signal and reference signal
- Knock detection using knock vs. reference comparison plus threshold
- Knock Output pin to signal outside circuits of knock detection results
- External clock inputs of 20, 24, 28, 32, 36, and 40 MHz
- SPI interface
- Operating Temperature Range of -40°C to + 125°C
- Operating Voltage of 5 ± 0.25 V

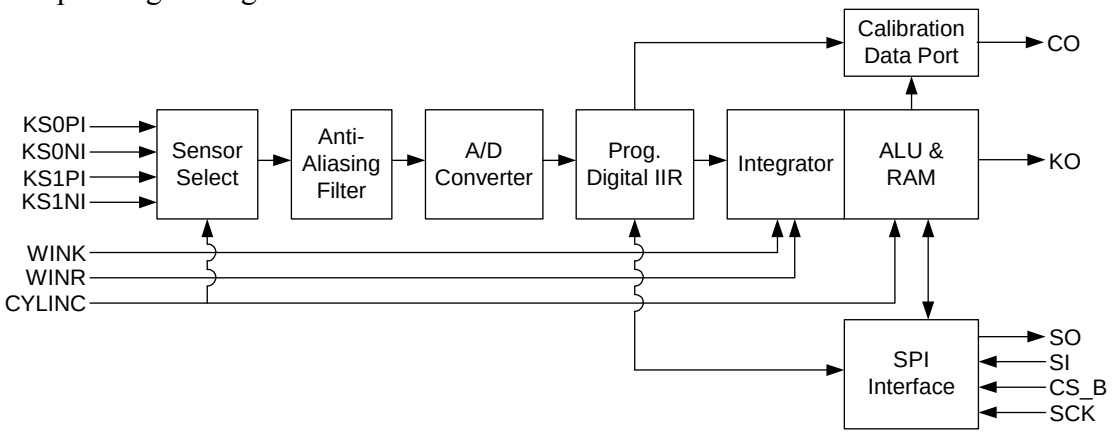


Figure 1.1 – Block Diagram of Prosak Knock System

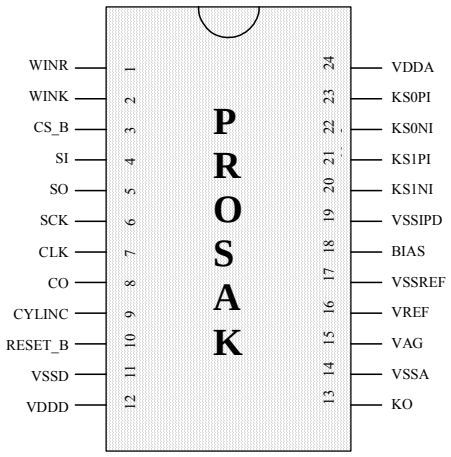


Figure 1.2 – Prosak IC, Top View

Pin #	Pin Name	Description
1	WINR	Reference Window – input for the reference integration window.
2	WINK	Knock Window – input for the knock integration window.
3	CS_B	SPI Chip Select Bar. (active low)
4	SI	SPI Serial data In.
5	SO	SPI Serial data Out.
6	SCK	SPI Serial ClocK input.
7	CLK	Clock. Main clock input for the chip
8	CO	Calibration Output. Used when calibrating knock
9	CYLINC	Cylinder Increment. Increments the cylinder sequence counter.
10	RESET_B	RESET. This pin should be tied to system reset.
11	VSSD	Digital VSS. Digital negative supply pin.
12	VDDD	Digital VDD. Digital positive supply pin.
13	KO	Knock Output. Digital output to indicate knock was detected, or indicates the knock calculation and/or reference calculation is valid.
14	VSSA	Analog VSS. Analog negative supply pin.
15	VAG	Analog Ground. Used internally for a bias point.
16	VREF	Voltage Calibration. Reference input for the Knock A/D converter. Connect to a precision 2.5 V voltage reference.
17	VSSREF	Voltage Ground Reference. Connect to the ground of the 2.5 V voltage reference.
18	BIAS	Bias Current. Used to set the bias current inside the IC.
19	VSSIPD	Input protection VSS. Negative supply for input protection networks.
20	KS1NI	Knock Sensor 1 Negative Input.
21	KS1PI	Knock Sensor 1 Positive Input.
22	KS0NI	Knock Sensor 0 Negative Input.
23	KS0PI	Knock Sensor 0 Positive Input.
24	VDDA	Analog VDD. Analog positive supply pin.

Table 1.1 – Pin Descriptions

DIMENSIONS

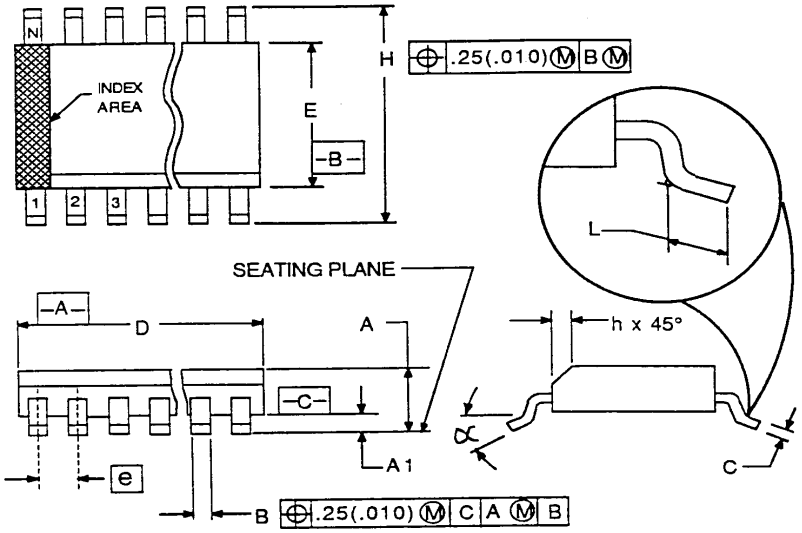


Figure 1.3 – Package Dimensions

Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	2.35	2.65	0.093	0.104
A1	0.10	0.25	0.004	0.009
B	0.35	0.49	0.014	0.019
C	0.25	0.32	0.010	0.012
D	15.25	15.50	0.601	0.610
E	7.40	7.60	0.292	0.299
N	24		24	
e	1.27 BSC		0.050 BSC	
H	10.05	10.55	0.395	0.415
h	0.25	0.75	0.010	0.029
L	0.50	0.90	0.020	0.035
α	0°	7°	0°	7°

Table 1.2 – Package Dimensions (related to Figure 1.3)

Notes: 1. Controlling Dimension: Millimeter
2. Dimension D and E do not include mold protrusion.

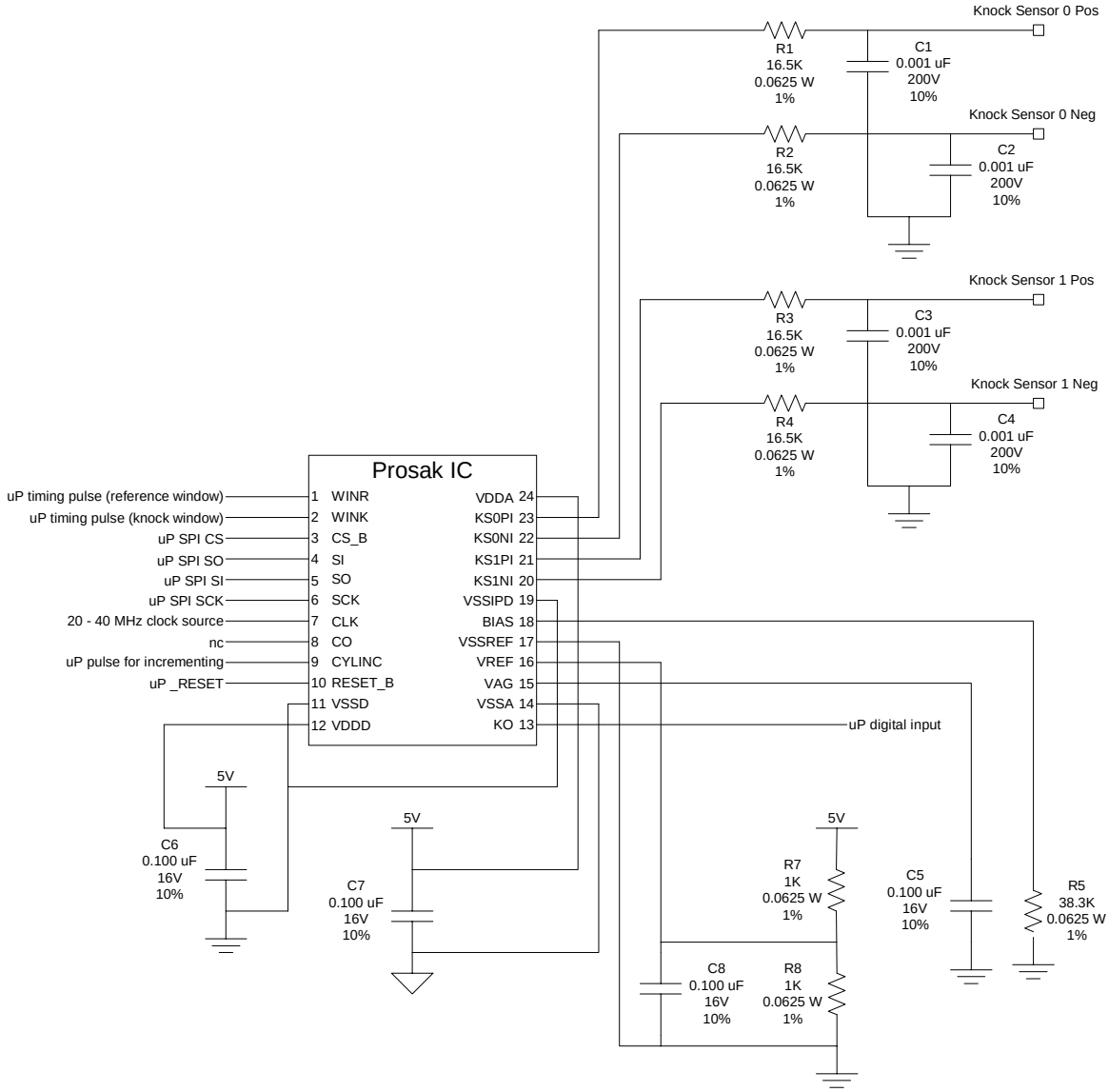


Figure 1.4 – Recommended Circuit Implementation*

* Notes:

1. For a single window system, pin 1 (WINR) should be grounded.
2. The above circuit shows 2 knock sensors. For a system utilizing a single knock sensor, pins KS1PI and KS1NI can be no connects or can be grounded.
3. It is recommended that if possible, a precision 2.5V reference should be used in place of the circuit shown for VREF.
4. The CO pin is shown as a no connect. This pin is not used in normal operation, however it is used in the custom calibration tools for the IC. See Appendix A.

1.2 Maximum Ratings

Characteristic	Symbol	Value	Unit
DC Power Supply Voltage	VDD	-0.3, 7.00	V
Maximum Supply Current	Idd	20	mA
Voltage from any pin to GND	Vin	-0.3, VDD+0.3	V
Storage Temperature Range	Tstg	-55, +150	ºC
Junction Temperature	Tj	150	ºC
Lead Temp. during solder (10 s)	Ts	260	ºC

Table 1.3 – Maximum Ratings

NOTE: Stress greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those listed in the following sections is NOT implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

1.3 SPI, CLK, and CYLINC Circuit Performance

ELECTRICAL CHARACTERISTICS [VDD = 5.0V ± 5%, T_A = -40 ºC to 125 ºC]

Characteristic	Symbol	Min	Typ	Max	Unit
SCK frequency	f_{sck}			8	MHz
SI setup time	T_{SIS}	30			ns
SI hold time	T_{SIH}	10			ns
SCK to SO valid time	T_{SOV}	0		75	ns
SCK Pulse Width	T_{CLKPW}	40	50	60	%
Delay after transfer: Normal Operation	DT	$7/f_{CLK}$			ns
Delay before SCK	DSC	0			ns
CS_B, SCK, and SI Input Voltage Threshold	V_{IH}	.7VDD			V
	V_{IL}			.3VDD	V
SO Output Drive	V_{OH}	VDD-0.05			V
		VDD - 0.4			V
	V_{OL}			0.05	V
				0.4	V
CLK frequency	f_{CLK}	20		40	MHz
CLK	Vih	.7VDD			V
	Vil			.3VDD	V
CYLINC Input	V_{IH}	.7VDD			V
	V_{IL}			.3VDD	V

Table 1.4 – SPI, CLK, and CYLINC Circuit Performance

1.4 Knock Circuit Performance

The specifications below are for the complete KNOCK circuit measured at the I/O pads of the IC. To include external components simply include the attenuation caused by the external resistor network.

ELECTRICAL CHARACTERISTICS [VDD = 5.0 V ± 5%, TA = -40 ºC to 125 ºC]

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Differential Input Impedance		KSxPI to KSxNI	416			kΩ
Input Leakage					100	nA
Common Mode Rejection			40			dB
Common Mode Bias Voltage				2.77		V
Input sampling rate				CLK / 128, 192, or 256		MHz
WINK and WINR Input	V_{IH}		.7VDD			V
	V_{IL}				.3VDD	V
Window Length					87	ms
KO Output Drive	V_{OH}	I_{LOAD} = 0 µA	VDD - .05			V
		I_{LOAD} = 250 µA	VDD - 0.4			V
	V_{OL}	I_{LOAD} = 0 µA			.05	V

Table 1.5 - Knock Circuit Performance

1.5 Calibration Output Circuit Performance

ELECTRICAL CHARACTERISTICS [VDD = 5.0V ± 5%, TA = -40 ºC to 125 ºC]

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
CO Output Drive	V_{OH}	I_{LOAD} = 0 µA	VDD-0.05			V
		I_{LOAD} = 250 µA	VDD - 0.4			V
	V_{OL}	I_{LOAD} = 0 µA			0.05	V
		I_{LOAD} = 2.5 mA			0.4	V

Table 1.6 - Calibration Performance

2. User Setup and Operation

The PROSAK IC processes data in the following manner (refer to Figure 1.1):

1. The sensor select block determines which knock sensor signal to pass through to the internal circuitry. The sensor is selected based on an on-chip cylinder counter.
2. The signal is passed through an anti-aliasing filter.
3. The output of the anti-aliasing filter is then over-sampled via a sigma-delta converter. The output of the converter is a 16-bit value which is updated at a rate determined by the internal clock frequency.
4. The sampled output is then passed through a programmable digital 8^{th} order IIR filter (implemented as 4 cascading 2^{nd} order filters).
5. During a knock window (WINK) or reference window (WINR), the absolute value of the output of the IIR filter is summed (integrated) and stored.
6. If desired, the PROSAK IC can be programmed for on-chip knock determination (binary condition of knock / no knock) with a digital output (KO) to signal an engine knock condition.

The values of the IIR filter coefficients are written to the PROSAK IC via the SPI interface. The values of the knock or reference signal integration can be read via the SPI interface for software calculation of knock if the user elects not to use the on-chip knock determination capabilities.

This section covers the software setup for each mode of operation of the PROSAK IC. Note that for each of the write registers described here, there is a corresponding read register to verify any information written to the IC if it is desirable for diagnostic purposes.

2.1.1 Single-Window Control

2.1.1.1 Initialization – Knock Determination via Software

The following steps must be taken to setup the IC via software at initialization.

1. Clock Setup: The internal clock must be set based on the external clock frequency supplied to the IC (see section 4). Address F1 (W-SETUP) must be set, but first the register must first be unlocked by sending information to address F0 (UNLOCK).
2. Cylinder Increment: The numbers of cylinders must be set via address F4 (W-CYLSETUP) (see section 5).
3. Sensor Select: The sensor numbers (0 or 1) corresponding to each cylinder number must be programmed at address E0 (W-KNKSS) (see section 6).
4. Filter Coefficients: The initial set of IIR filter coefficients must be programmed into the IC at addresses 80-93 (W-KNKCOEF) (see section 6).
5. Knock Setup: The setup for the knock system at address F7 (W-KNKSETUP1) must be set with the following actions (see section 6):
    a. Enable the IIR filter
    b. SSCHG set to 0. This changes the sensor select after knock calculation window, since there is no reference window.
    c. KOSEL should be set to 000.
    d. Set the other parameters in this register as needed for the application.

2.1.1.2 Initialization – Knock Determination On-Chip

In addition to be above initialization components, the following steps must be taken to setup the IC via software at initialization when on-chip knock processing. All registers are found in section 6 of this document. If the knock determination is made via software, these steps are not needed.

1. Thresholds: Set each cylinder threshold at addresses C0 – CB (W-KNKTHR0-11).
2. Reference Average: Write the reference averages to be used at addresses D0 (W-REFA0H), D1 (W-REFA0L), D2 (W-REFA1H), and D3 (W-REFA1L). These must be set since there is no updating of reference information automatically in single-window mode.
3. Knock Setup: The setup for the format of knock scale must be set at address F6 (W-KNKSETUP0).
4. Knock Setup: The setup for the knock system at address F7 (W-KNKSETUP1) must be set with the following actions (see section 6):
    a. Enable the IIR filter
    b. SSCHG set to 0. This changes the sensor select after knock calculation window, since there is no reference window.
    c. KOSEL must be set to 001.
    d. Set the other parameters in this register as needed for the application.

2.1.1.3 Synchronization

Upon synchronization of the engine, address F3 (W-CYLSYNC) must be set (see section 5).

2.1.1.4 Engine Operation

Depending on the application and calibration of an engine, it may be desirable to change the filter coefficients at different engine operating points. To do this, first disable the IIR filter by accessing address F7 (W-KNKSETUP1), update the IIR coefficients at addresses 80-93 (W-KNKCOEF), then re-enable the IIR filter by accessing address F7 (W-KNKSETUP1).

It may be desirable to check for overflows of the IIR filter periodically via address 78 (R-KKNKSTAT0).

If the knock determination is being made on-chip, then the thresholds at addresses C0 – CB (W-KNKTHR0-11) and the reference averages at addresses D0 (W-REFA0H), D1 (W-REFA0L), D2 (W-REFA1H), and D3 (W-REFA1L) may also be changed at any time.

2.1.2 Dual-Window Control

2.1.2.1 Initialization – Knock Determination via Software

The following steps must be taken to setup the IC via software at initialization.

1. Clock Setup: The internal clock must be set based on the external clock frequency supplied to the IC (see section 4). Address F1 (W-SETUP) must be set, but first the register must first be unlocked by sending information to address F0 (UNLOCK).
2. Cylinder Increment: The numbers of cylinders must be set via address F4 (W-CYLSETUP) (see section 5).

3. Sensor Select: The sensor numbers (0 or 1) corresponding to each cylinder number must be programmed at address E0 (W-KNKSS) (see section 6).
4. Filter Coefficients: The initial set of IIR filter coefficients must be programmed into the IC at addresses 80-93 (W-KNKCOEF) (see section 6).
5. Knock Setup: The setup for the knock system at address F7 (W-KNKSETUP1) must be set with the following actions (see section 6):
    a. Enable the IIR filter
    b. Set the SSCHG based on the desired window sequence
    c. KOSEL should be set to 000.
    d. Set the other parameters in this register as needed for the application.

2.1.2.2 Initialization – Knock Determination On-Chip

In addition to be above initialization components, the following steps must be taken to setup the IC via software at initialization when on-chip knock processing. All registers are found in section 6 of this document. If the knock determination is made via software, these steps are not needed.

1. Thresholds: Set each cylinder threshold at addresses C0 – CB (W-KNKTHR0-11).
2. Reference Average Filtering: Set the filters used for the reference average at addresses CC (W-KNKCNU), CD (W-KNKCND), CE (W-KNKCKU), and CF (W-KNKCKD).
3. Knock Setup: The setup for the format of knock scale must be set at address F6 (W-KNKSETUP0).
4. Knock Setup: The setup for the knock system at address F7 (W-KNKSETUP1) must be set with the following actions (see section 6):
    a. Enable the IIR filter
    b. Set the SSCHG based on the desired window sequence
    c. KOSEL must be set to 001.
    d. Set the other parameters in this register as needed for the application.

2.1.2.3 Synchronization

Upon synchronization of the engine, address F3 (W-CYLSYNC) must be set (see section 5).

2.1.2.4 Engine Operation

Depending on the application and calibration of an engine, it may be desirable to change the filter coefficients at different engine operating points. To do this, first disable the IIR filter by accessing address F7 (W-KNKSETUP1), update the IIR coefficients at addresses 80-93 (W-KNKCOEF), then re-enable the IIR filter by accessing address F7 (W-KNKSETUP1).

It may be desirable to check for overflows of the IIR filter periodically via address 78 (R-KKNKSTAT0).

3. Serial Peripheral Interface

The SPI is the main communication system on the PROSAK IC. It allows the microcontroller unit (MCU) to communicate with the PROSAK IC as a 16 bit SPI slave device.

The MCU initiates a SPI transfer by asserting the slave select line connected to the CS_B (Chip Select Bar) pin on the PROSAK IC. Data is simultaneously received (shifted in serially from the MCU on the SI pin) and transmitted (shifted out serially to the MCU on the SO pin). The data that is transmitted out on SO is in response to the command that was received on SI the previous time the MCU communicated with the PROSAK IC. A serial clock line (SCK) synchronizes shifting and sampling of information on the two serial data lines.

The SPI allows the MCU to read data out of all the registers located in the PROSAK IC. After receiving a request from SPI on the SI pin, the corresponding data is loaded to the shift register and transferred serially through the SO pin when the next transmission is made.

3.1 Implementation of the Serial Peripheral Interface

This section deals with the operation of the SPI, and command structure used by the SPI.

3.1.1 Operation of the SPI

3.1.1.1 SPI: Single 8 Bit and Single 16 Bit Mode

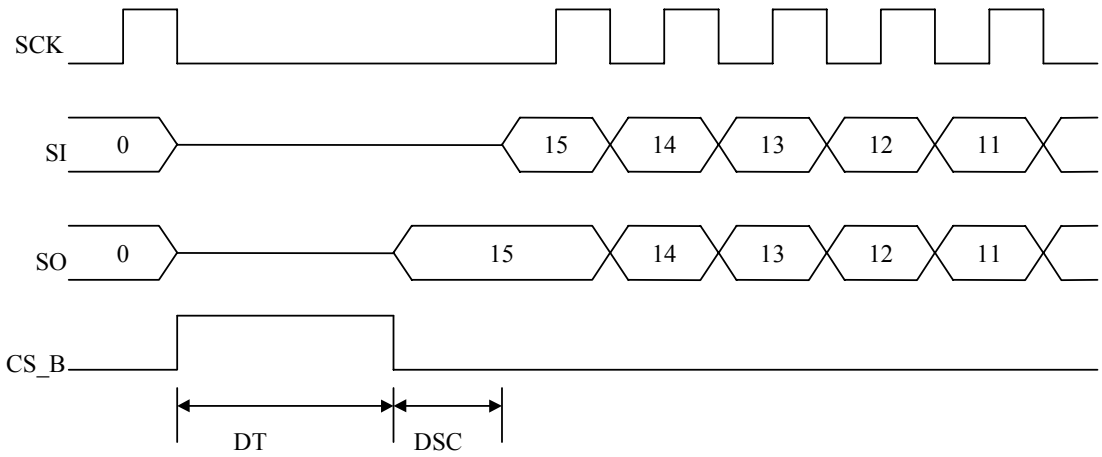


Figure 3.1 - SPI Transfer Timing Diagram

As shown in Figure 3.1, when the CS_B pin is high, the SPI is idle and no communication is taking place over the SI and SO pins. The serial interface stays in the idle state until it detects that the PROSAK is being selected by the MCU (CS_B is asserted). The MCU generates SCK, which the SPI uses to shift the data from the MCU into the SI pin and shifts the response to the previous command out the SO pin. After 16 SCKs, the PROSAK decodes the command that was received on the SI pin. The PROSAK then writes the data to the selected register (if the register is a write register) and always reads the data of the selected register to get ready for the next transfer.

In order to assure a successful SPI data transfer, certain timing restrictions must be observed by the MCU. These timing restrictions are listed in Table 1.4 and described here. As shown in Figure 3.1, once CS_B is negated, it must remain high for a certain period of time known as DT (Delay after Transfer). Once CS_B is asserted, there must be a delay specified by DSC (Delay until Serial Clock) before SCK begins.

3.1.1.2 SPI: Block Mode

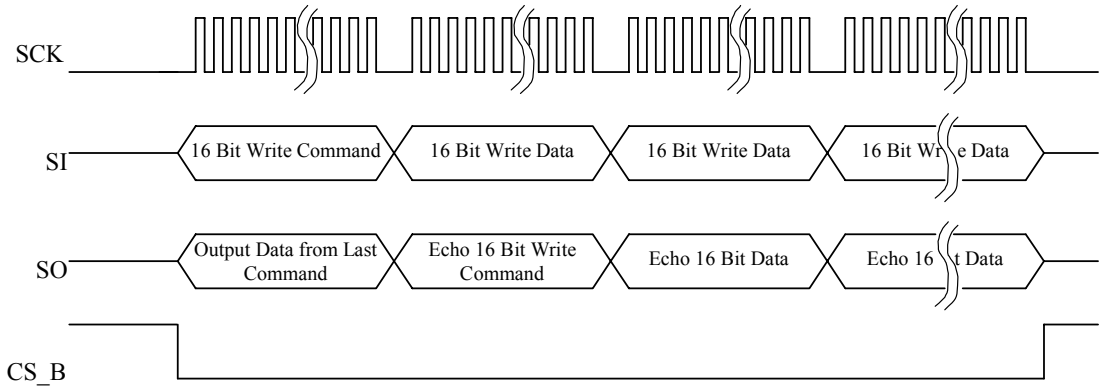


Figure 3.2 - SPI Transfer Block Write Timing Diagram

Figure 3.2 shows the SPI transfer timing diagram for a block write. During block write transfers, the PROSAK can be written with blocks of 16 bit data. The first 16 bits after CS_B is asserted define the starting address to which the next 16 bit block of data received on SI will be written. The following 16 bit data blocks will be written in consecutive locations. After every 16 bit transfer, the data will be written on the data bus. The 16 bit frames will be interpreted as data until CS_B is negated.

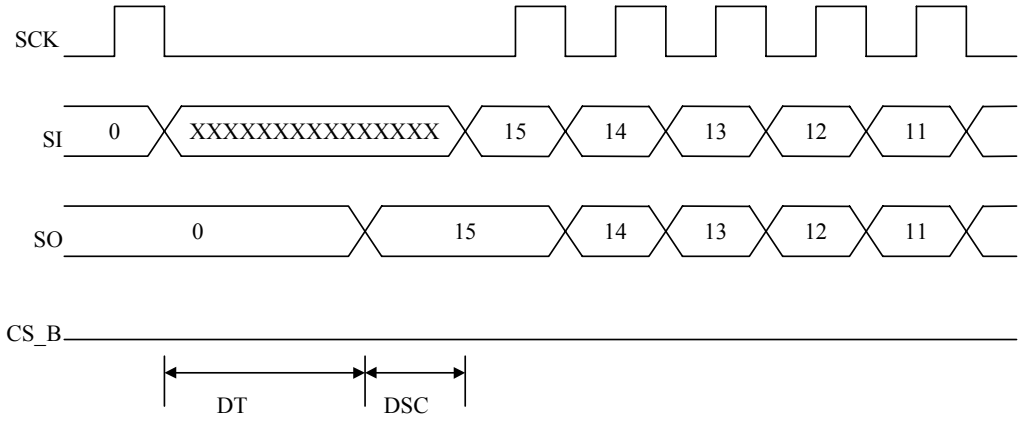


Figure 3.3 - SPI Transfer Block Write Timing Diagram with Timing Restrictions

In order to assure a successful SPI data transfer, certain timing restrictions must be observed by the MCU. These timing restrictions are listed in Table 1.4 and described here. As shown in Figure 3.3, DT refers to the time that elapses between the falling edge of the 16th SCK, and the

most significant bit of the output data being shifted out of SO. Once DT has elapsed, there must be a delay specified by DSC (Delay until Serial Clock) before SCK begins.

3.1.2 Serial Interface Command Structure

There are three types of write commands (single 8 bit data, single 16 bit data, and multiple 16 bit data) and one type of read command for the PROSAK IC. The write commands are used to modify registers in the PROSAK IC, for example setup registers or KNOCK programmable filter coefficients. The write commands automatically cause a read of the register being written, which is shifted out on SO in the next frame. The read command is use to read registers. All data transfers out of the SO pin are 16 bits.

3.1.2.1 SI-SO Relationship

The SPI shifts data in (SI) and out (SO) simultaneously. However, a response to a command is always delayed by one SPI transfer (i.e. response to the command N is shifted out at the same time command N+1 is shifted in).

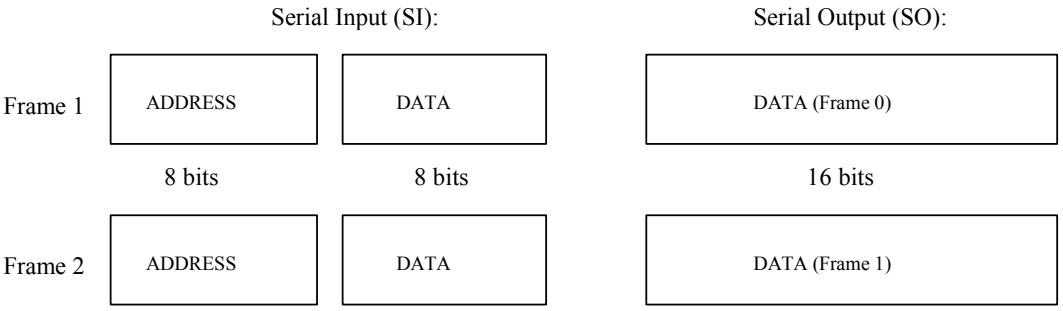


Figure 3.4 - Example of SPI SI-SO relationship

3.1.2.2 Single 8 bit data write

A typical SPI write consists of one 16 bit frame. The frame transmitted by the CPU, into the SI pin, consists of 8 command bits and 8 data bits. The PROSAK returns 16 data bits on SO from the previously sent command. The CS_B pin of the PROSAK IC must be asserted for all 16 bits. Note, the upper 16 locations are reserved for 8 bit register writes (F0H-FFH).

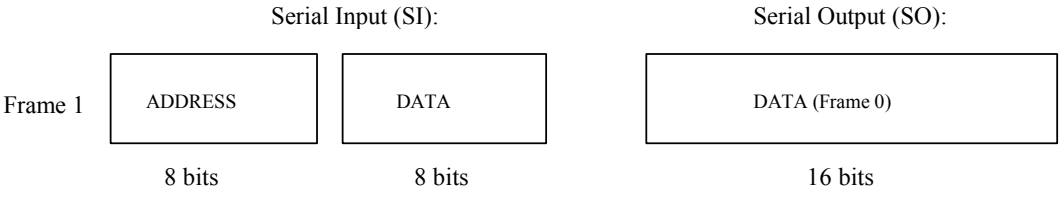


Figure 3.5 - Single 8-bit SPI Write Format

3.1.2.3 Single 16 bit data write

112 lower address locations (80H – EFH) are reserved for registers requiring more than 8 bits of data to be written to the PROSAK. These 112 addresses use the same address bits as the 8 bit data write, and the 16 data bits must follow in the next SPI transfer. The CS_B pin must be asserted continuously for both frames. In this case the PROSAK echoes the command out of SO in the second frame while the 16 bit data is being shifted in on SI.

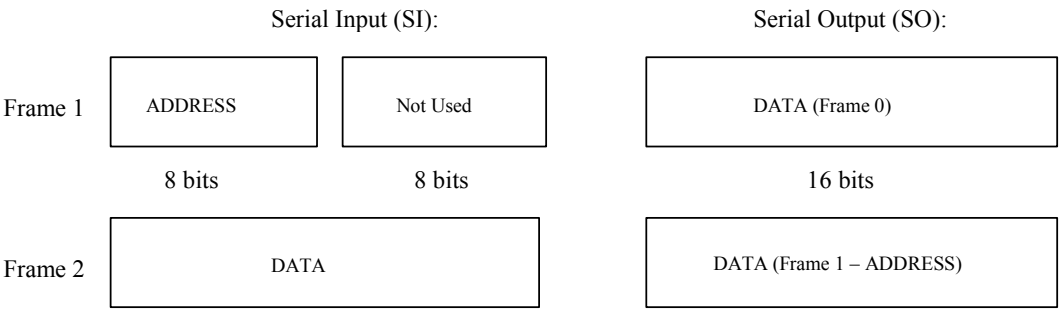


Figure 3.6 - Single 16 bit SPI Write Format

3.1.2.4 Block 16 bit data write

The 112 lower address locations (80H – EFH) access various sets of coefficients for the Knock functions. It may be convenient to write the continuous locations at once. This is accomplished by following the same procedure as the single 16 bit write, and continuing to send in the consecutive 16 bit data words while keeping CS_B asserted. This alleviates the overhead of sending address and data for each location, by sending the starting address followed by multiple data. Negating CS_B terminates multiple 16 bit writes. All of the 16 bit words up to the time CS_B is negated will be written. If CS_B is negated in the middle of a 16 bit word, the partially transmitted word will be ignored.

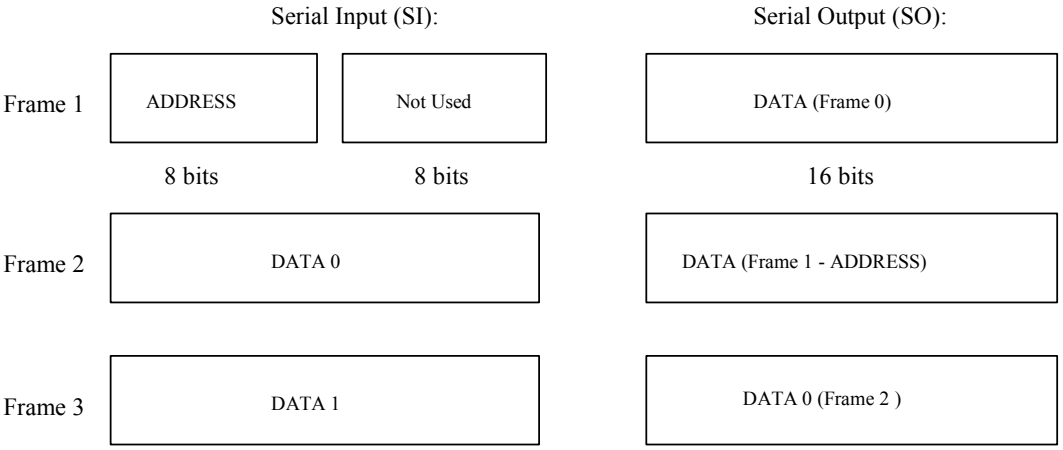


Figure 3.7 - Multiple 16 bit SPI Write Format

3.1.2.5 Read

A SPI read is used to read the registers in the PROSAK. The command transmitted by the CPU into the SI pin consists of 8 command bits and 8 don't care. The PROSAK returns 16 data bits on SO from the previously sent command. During the next frame transmitted by the CPU, the requested data from the PROSAK IC is shifted out of the SO pin. If no other data is immediately needed from the PROSAK, a NOP command may be sent in on SI to flush the requested data out of the SO pin. A NOP command is address 72 followed by 8 don't care bits to complete the 16-bit SPI message. The NOP will return zeros.

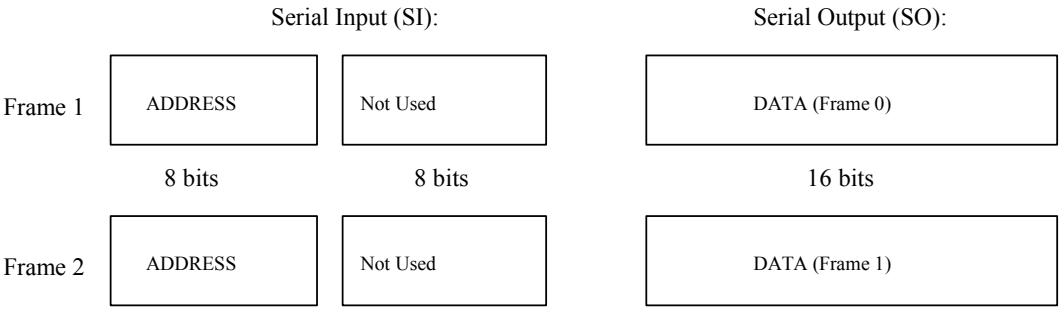
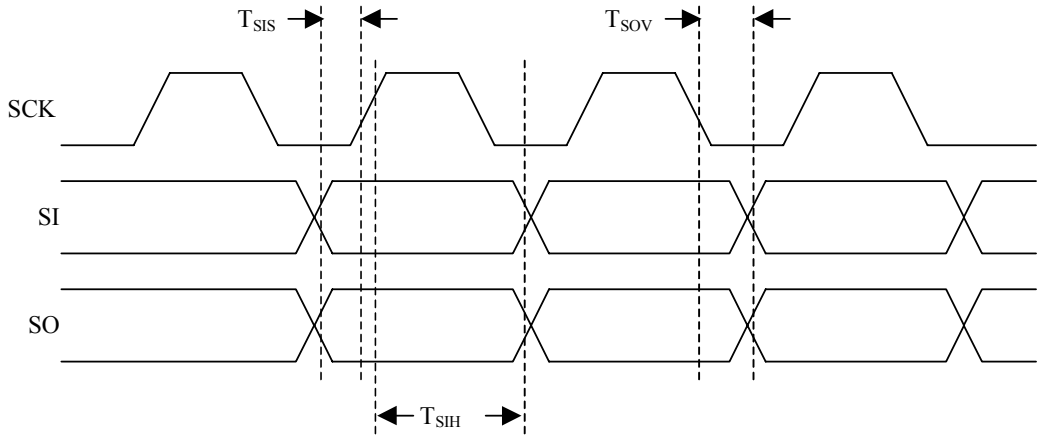


Figure 3.8 - SPI Read Format (any size data)



NOTE:
All timing is shown with respect to 30% VDD and 70% VDD.

Figure 3.9 - SI and SO Timing

4. Internal Clock Generator

In order to save a crystal oscillator, all the clocks on the PROSAK IC are derived from the CLK pin. A programmable divider divides the CLK pin to generate the internal clocks. The allowable CLK pin frequencies (f_{CLK}) are 20, 24, 28, 32, 36, and 40 MHz. The internal clocks derived from the CLK pin are the knock modulator clocks.

The internal clock is generated by dividing the CLK pin by 128, 192, or 256. The divide-by ratio for the clock is controlled by the SETUP-0 register MODCLKF field. The modulator clock frequency must be configured per Table 4.1 for functionality of the Knock Circuit to be guaranteed.

CLK Frequency f_{CLK} (MHz)	MODCLKF (values in hex)	Divide by Ratio	Internal Clock Frequency (kHz)
40	0	256	156.3
36	1	192	187.5
32	1	192	166.7
28	1	192	145.8
24	2	128	187.5
20	2	128	156.3

Table 4.1 - Modulator Clock Divider Setup

4.1 Internal Clock Generator Registers

Address (71) R-SETUP – Read Setup Register		
Bit #	Data from PROSAK	Reset
15-2	Unused	0
1-0	MODCLKF – These two control bits define the divide by rate that generates the internal clock from the CLK pin. 00 – Divide by 256 01 – Divide by 192 10 – Divide by 128 11 – Divide by 192	0
This register is used to configure the core functions of the PROSAK IC.		

Address (F0) W-UNLOCK – Write Unlock Register		
Bit #	Data to PROSAK	Reset
15-8	Address (F0)	0
7-0	Unlock Word = CA	0
This register is used to unlock the SETUP register. To modify the SETUP register, a write with the correct unlock word of CA must directly proceed a write to the SETUP register.		

Address (F1) W-SETUP – Write Setup Register		
Bit #	Data to PROSAK	Reset
15-8	Address (F1)	0
7-2	Unused	0
1-0	MODCLKF – These two control bits define the divide by rate that generates the internal clock from the CLK pin. 00 – Divide by 256 01 – Divide by 192 10 – Divide by 128 11 – Divide by 192	0
This register is used to configure the core functions of the PROSAK IC. To write this register, a write to the UNLOCK register with the correct unlock data word must directly proceed the write to this register.		

5. Cylinder Increment

The cylinder circuit is a four bit counter that keeps track of the next cylinder that is to fire. The cylinder counter will count from zero to the number of cylinders-1. The counter will increment on every rising edge of the CYLINC signal. The counter can be synced to the correct cylinder by writing to the cylinder sync register.

The register CYLSETUP defines how many cylinders are configured, and the value to synchronize the counter to.

5.1 Implementation of the Cylinder Circuit

The counter will count from 0 to the value defined in MAXCYL. MAXCYL in the CYLSETUP register is the number of cylinders-1. The allowable number of cylinders is from 1 to 12. The counter will allow any number of cylinders from 1 to 16, but the knock circuit only supports from 1 to 12 cylinders.

The counter will be modified on every rising edge of CYLINC. If the value of the counter equals the value stored in MAXCYL, then on the next rising CYLINC edge, the counter will be loaded with 0, otherwise the counter will be loaded with the last counter value plus one.

The counter can be synchronized to the correct cylinder value by initializing the SYNCCYL field in the W-CYLSYNC register with the value to synchronize the counter to, and set the SSYNCCYL field in the W-CYLSYNC register to ‘1’. When the W-CYLSYNC register is written with the SSYNCCYL field bit set to ‘1’, an internal flag will be set. This flag will indicate that on the next rising CYLINC edge, the value stored in the SYNCCYL field will be loaded into the counter, and the internal flag will be cleared.

5.2 Cylinder Registers

Address (73) R-CYLSYNC – Read Sync Cylinder Register		
Bit #	Data from PROSAK	Reset
15-4	Unused	0
3-0	SYNCCYL – These 4 bits define the cylinder - 1 number that will be loaded into the cylinder counter when the SSYNCCYL bit has been written to a '1', and a rising CYLINC edge is detected.	0
This register returns the value that was last written in the SYNCCYL field.		

Address (74) R-CYLSETUP –Read Cylinder Setup Register		
Bit #	Data from PROSAK	Reset
15-8	Unused	0
7-4	CYLVAL – These 4 bits define the current cylinder value.	0
3-0	MAXCYL – These 4 bits define the number of cylinders – 1 that will be used. The Knock circuit supports only values from 0 to 11.	0
This register controls the setup and operation of the cylinder counter.		

Address (F3) W-CYLSYNC – Write Sync Cylinder Register		
Bit #	Data to PROSAK	Reset
15-8	Address (F3)	0
7-5	Unused	0
4	SSYNCCYL – When this bit is written to '1', will set an internal flag that will indicate that during the next rising CYLINC edge, load the counter with the SYNCCYL field.	0
3-0	SYNCCYL – These 4 bits define the cylinder - 1 number that will be loaded into the cylinder counter when the SSYNCCYL bit has been written to a '1', and a rising CYLINC edge is detected.	0
This register will sync the cylinder counter to the engine using the SYNCCYL value on the next edge of CYLINC pin, if the SSYNCCYL field is written to a 1.		

Address (F4) W-CYLSETUP –Write Cylinder Setup Register		
Bit #	Data to PROSAK	Reset
15-8	Address (F4)	0
7-4	Unused	0
3-0	MAXCYL – These 4 bits define the number of cylinders that will be used. Values may be 0 to 11 inclusive.	0
This register controls the setup and operation of the cylinder counter.		

6. Knock Detection

This section defines the electrical and DSP implementation of the knock. The knock system consists of the following components (refer to Figures 1.1 and 1.4):

1. Knock sensor interface - differential input pairs KS0PI/KS0NI and KS1PI/KS1NI
2. Sensor select
3. Anti-aliasing filter
4. A/D converter
5. Programmable IIR filter
6. Integrator
7. ALU & RAM
8. Knock output (KO)

6.1 Knock Sensor Interface

The broadband (or linear) sensor is modeled as a voltage source with a series capacitance and a resistance between the output connections. The recommended external RC network is shown in Figure 1.4.

6.2 Sensor Select

This stage allows selection of one of the two sensor inputs, either KS0PI/KS0NI or KS1PI/KS1NI, for each cylinder. The KNKSS register is used to select which knock sensor (either 0 or 1) will be used with each of twelve possible cylinders (from 0 to 11). The KNKSS register is used to read the status of the knock sensor select register.

For each cylinder, it is possible that the knock window be placed either before or after the reference window. In order for the Sensor Select to change sensors for the new cylinder, it must know the order of the knock and reference windows. SSCHG field in the KNKSETUP1 register accomplishes this by programming the sensor change to occur after either the knock window (0), or the reference window (1).

6.3 Anti-Aliasing Filter

The internal second order lowpass anti-aliasing filter is designed such that there is less than 1 dB of attenuation at frequencies below 25 kHz, and more than 50 dB of attenuation above the effective sampling rate.

6.4 A/D Converter

The A/D converter has unity gain by default. With unity gain, the converter can take inputs signals as large as ±2.5V (for VDD = 5.0V). If the input signals are within the range of ±1.25V (for VDD = 5.0V), the gain can be increased to two. This is done by setting KNKGAIN in the KNKSETUP1 register to a 1. (The default setting of KNKGAIN is 0, which results in unity gain on the converter).

6.5 Programmable IIR Filter

The digital programmable filter is a digital 8th order IIR filter. The programmable filter is implemented as a cascade of four digital biquads as shown in Figure 6.1. Each biquad can handle up to two poles and two zeros so that the entire filter can handle filter designs up to eight poles and eight zeros.

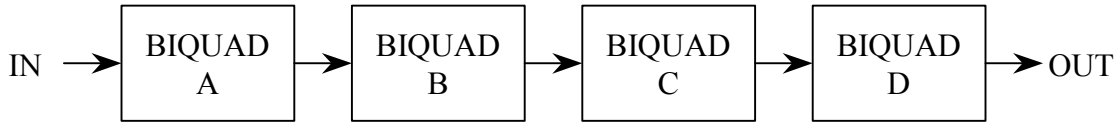


Figure 6.1 - System Flow Graph for Knock Digital IIR Filter

The filters have the form:

$$H(z) = \frac{b_{0A}+b_{1A}z^{-1}+b_{2A}z^{-2}}{1+a_{1A}z^{-1}+a_{2A}z^{-2}} \times \frac{b_{0B}+b_{1B}z^{-1}+b_{2B}z^{-2}}{1+a_{1B}z^{-1}+a_{2B}z^{-2}} \times \frac{b_{0C}+b_{1C}z^{-1}+b_{2C}z^{-2}}{1+a_{1C}z^{-1}+a_{2C}z^{-2}} \times \frac{b_{0D}+b_{1D}z^{-1}+b_{2D}z^{-2}}{1+a_{1D}z^{-1}+a_{2D}z^{-2}}$$

Note:
b_{0A} represents the b_0 numerator coefficient for biquad A
a_{2D} represents the a_2 denominator coefficient for biquad D

Twenty total coefficients (five per biquad) are downloaded via SPI commands. Each coefficient is a 14-bit number limited to the range between -4.0 and +4.0. The coefficients must be downloaded to the PROSAK chip in sign-magnitude format into the KNKCOEFF registers. Reading the KNKCOEFF registers will output the last written filter coefficients.

The normal operation of the filter includes the following steps:

1. Program the filter coefficients.
2. Enable the filter with the IIRENABLE bit in the KNKSETUP1 register.
3. Wait for the transients of the step response to settle.
4. Begin an integration interval.

Whenever the user changes sensor inputs, the filter is reset. It is possible to change the filter response while in operation by clearing the IIRENABLE bit in the W-KNKSETUP1 register, and

then changing the filter coefficients. After the coefficients are altered, the IIRENABLE bit must be asserted and the filter will be reset.

6.6 Integrator

This stage performs two independent integrations of the filter output. The WINK and WINR windowing signals determine the duration of the integration. The integrators are 32 bit accumulators that are updated at the IIR filter rate (internal clock rate from Section 3). If the integrators overflow, the individual overflow flags will be set in the KNKSTATUS0 register.

6.7 Knock Detect

The Knock Detect circuit provides an output to indicate when knock has occurred. The knock detect block calculates the knock intensity and generates a knock output after the knock window and calculates the reference average after the reference window. A separate reference average is stored for each sensor.

6.7.1.1 Knock Cylinder Sampling

The Knock Detect supports one threshold per cylinder, and supports independent sensor select on a per cylinder basis. The Knock Detect block will sample the cylinder counter at the end of the knock window based on the value in the KNKSETUP register. The sampled value will be stored in the KNKCYL field of the KNKSTATUS1 register. The Knock Detect will use KNKCYL field to select the threshold register to use (KNKTHR0-11) during the knock intensity calculation. The KNKCYL field will also be used to index into the KNKSS register to pick the correct sensor.

Figures 6.2 and 6.3 illustrates the knock cylinder counter system. The rising edge of CYLINC pin is the increment for the CYLCNT value, and will frame the current cylinder processing. The KNKCYL value is usually one cycle count behind the CYLCNT value as illustrated in the following figures. Note that the KNKCYL counter will be used to pick the threshold values, and the knock threshold values should account for this. In the examples below, during cylinder 2 processing, KNKTHR1 values will be accessed.

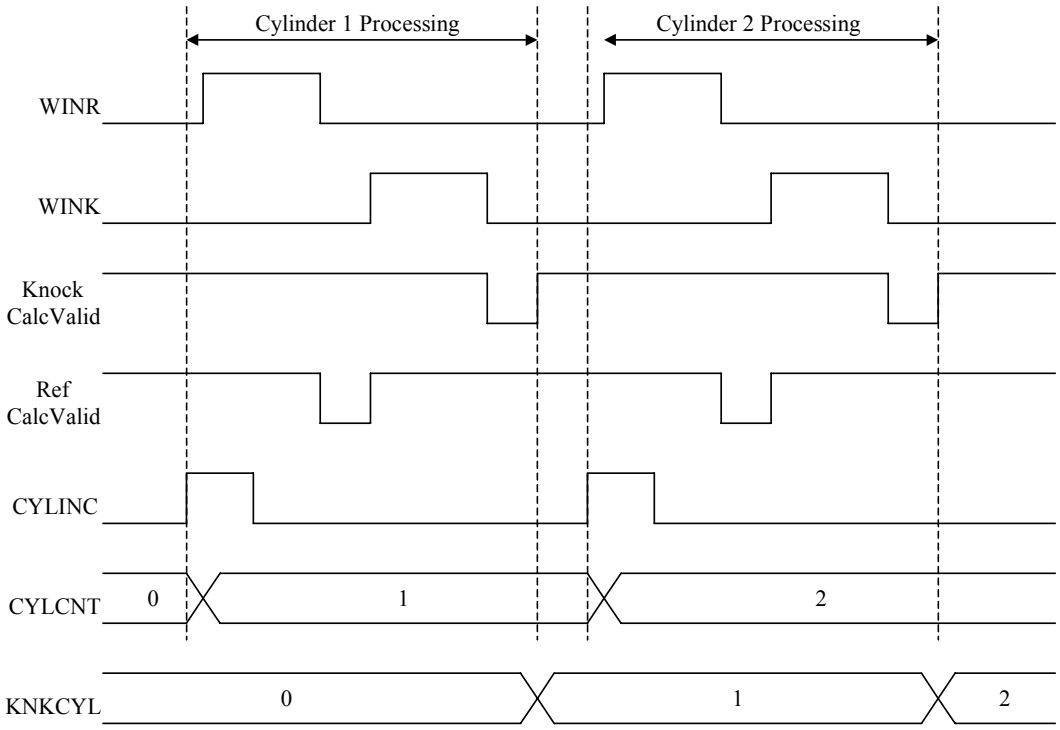


Figure 6.2 - KNKCYL Sequence Example With SSCHG=0

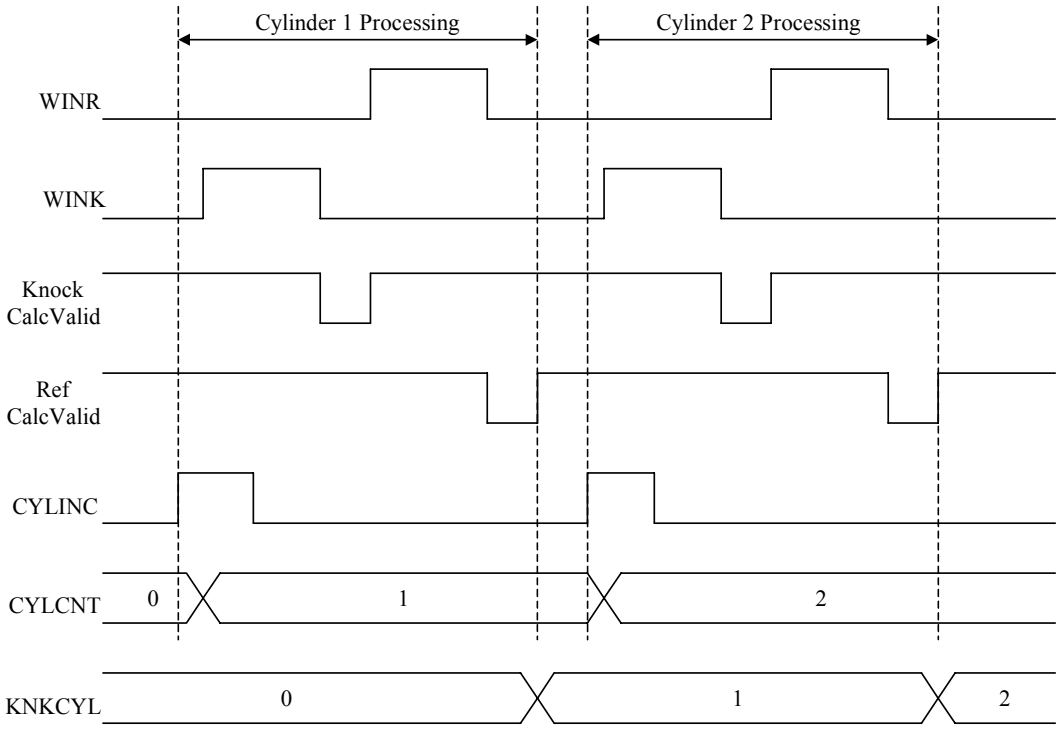


Figure 6.3 - KNKCYL Sequence Example With SSCHG=1

6.7.1.2 Reference Calculation

The background noise of the system is measured and integrated during the reference window and filtered in the Knock Detect block. The PROSAK supports two sensors, which requires two reference average values to be saved, one for each sensor.

After the falling edge of the reference window, the reference integration is presented to the Knock Detect block. The Knock Detect block will pass the reference integration value through a first order digital low pass filter to generate a new reference average. The filter calculates the reference average using the follow equation:

$$REF_{avgn} = C \times (REF_n - REF_{avgn-1}) + REF_{avgn-1}$$

The REF_{avgn-1} is the last calculated reference average for the current sensor. REF_n is the reference integration valued measured during the reference window. C is a fractional filter coefficient, which is always less than 1. The reference values (REF_{avg}) are stored in the REFA0H, REFA0L, REFA1H, and REFA1L registers.

In order to add flexibility and increase the performance of the filter's tracking capability, four coefficients can be used for the filter coefficient C. The coefficient C is programmable and is switched dynamically. If the filter is averaging up, one of two up averaging coefficients (C_{nu} and C_{ku}) is used. If the filter is averaging down, one of two down averaging coefficients (C_{nd} and C_{kd}) is used. Whether a knock occurred prior to the current reference integration determines which of the two up or down averaging coefficients is used. If knock occurred, C_{kd} or C_{ku} is used and if no knock occurred C_{nd} or C_{nu} is used. The up and down coefficients are used to help the filter track changes in the average reference level during such transient events. The knock coefficient can be used to slow the filter down to the extent that the current sample has hardly any effect on the average. The C_{nu}, C_{ku}, C_{nd}, and C_{kd} coefficients are stored in the KNKCNU, KNKCKU, KNKCND, and KNKCKD registers.

The Reference Calculation will be performed in the following order, and the bit lengths are described in Table 6.1:

$$DELTA = (REF_n - REF_{avgn-1})$$
$$NTEMP = (C \times DELTA)$$
$$REF_{avgn} = (NTEMP + REF_{avgn-1})$$

Name	Description	Bit Representation
REF_n	32 bit unsigned reference integration value	bbbbbbbbbbbbbbbbbbbbbbbbbbbbbb.
DELTA	33 bit signed delta	sbbbbbbbbbbbbbbbbbbbbbbbbbbbbbb.
C	16 bit unsigned fractional coefficient	0.bbbbbbbbbbbbbbb
NTEMP	33 bit signed result	sbbbbbbbbbbbbbbbbbbbbbbbbbbbbbb.
REF_{avg}	32 bit unsigned reference average	bbbbbbbbbbbbbbbbbbbbbbbbbbbbbb.

Table 6.1 - Reference Calculation Bit Representation

6.7.1.3 Knock Calculation

The knock signal is measured and integrated during the WINK knock window. The knock ratio and intensity are calculated in the Knock Detect block. The PROSAK supports twelve threshold values, one for each cylinder to be used in the knock intensity calculation.

After the falling edge of the knock window, the knock integration value is sent to the Knock Detect block. The knock integration is used to calculate the knock intensity using the following equation:

$$\text{Knock Intensity} = \frac{\text{KNOCK}}{\text{REF}_{avg}} - \text{Threshold}$$

The threshold is selected based on cylinder to allow individual thresholds per cylinder. If the result of the knock intensity calculation is less than zero, the knock intensity is set to zero. The Ratio of KNOCK Integration value to the reference average is stored in the KNKR register. The Knock Intensity value is stored in the KNKI register. The thresholds are stored in the KNKTHR0-11 registers.

The Knock Calculation will be performed in the following order:

$$\text{KNKR} = \frac{\text{KNOCK}}{\text{REF}_{avg}}$$
$$\text{KNKI} = (\text{KNKR} - \text{KNKTHR})$$

KNOCK is the 32 bit unsigned knock integration value, and REF_{avg} is the 32 bit unsigned reference average for the current cylinder. KNKR is the 16 bit unsigned ratio of the knock to reference. There is overflow logic to detect when the divider overflows. This output is visible through the calibration output and the KNKSTATUS1 register. If the KNKI operation generates a negative number, then the KNKI field is reported as zero.

The KNKSCALE field in the KNKSETUP0 register defines the format of KNKR, KNKI, and KNKTHR0-11. KNKSCALE determines where the decimal point is placed in these fields.

Depending on the ratio of the knock to reference window widths, the user may want to move the decimal point. For large ratios, it would be desirable to have the decimal point more to the right. For small ratios, it would be desirable to have the decimal point more to the left. By default, the decimal point is in the middle of the word. The KNKSCALE is set via address F6.

6.7.1.4 Knock/Reference Calculation Times

The KNOCKVAL flag in the KNKSTAT1 register defines when the KNKI and KNKR values are valid. During knock calculations, the KNOCKVAL flag will be cleared to indicate that new KNKI and KNKR values are being computed. The knock calculations begin after the falling edge of the knock window, and will complete after $200/f_{CLK}$.

The REFVAL flag in the KNKSTAT1 register defines when the reference average value is valid. During reference calculations, the REFVAL flag will be cleared to indicate that the new reference value is being computed. The reference calculations begin after the falling edge of the reference window, and will complete after $260/f_{CLK}$.

If the knock window falls while the reference calculations are computing, then the knock calculations will not start until the reference calculations are complete. If the reference window falls while the knock calculations are computing, then the reference calculations will not start until the knock calculations are complete. If both windows fall at the same time, the knock calculations will complete first, followed by the reference calculations.

6.7.1.5 KO Output Modes

The KO output pin can be programmed to indicate different Knock Detect Status. The KOSEL field in the KNKSETUP register defines what mode the KO pin will operate.

6.7.1.6 Knock Detect Status

The KNKSTATUS register gives the processor visibility into the Knock Detect block. The KNKCYL field in the KNKSTATUS register will report what cylinder is being processed by the Knock Detect block. The KIFLG field reports whether the KNKI is greater than zero. The KNOCKVAL field indicates that the KNKI and KNKR values are valid. The REFVAL field indicates that the REFAx values are valid. The status register also reports the IIR overflow flags the knock and reference integrator overflow flags, and the Knock Detect divide overflow flags. These overflow flags are set upon the error condition, and will hold their values until the processor reads the registers, then writes to the register with a zero in the overflow bit position to clear the flag.

KOSEL (binary)	Description
000	DISABLE - KO output pin disabled.
001	KIFLG – When the KNKI is greater than zero, the KO output will go high and remain high until the next knock calculation. When the KNKI zero, the KO output will go low and remain low until the next knock calculation.
010	KNOCKVAL – The KO pin will be high when the knock results are valid, and go low when the knock calculations are taking place and the KNKI and KNKR values are invalid.
011	KIFLG or KNOCKVAL – This is the logical or of the KIFLG and KNOCKVAL fields.
100	REFVAL – The KO pin will be high when the reference results are valid, and go low when the reference calculations are taking place and the REFAx values are invalid.
101	KIFLG or REFVAL – This is the logical or of the KIFLG and REFVAL fields.
110	KNOCKVAL or REFVAL – This is the logical or of the KNOCKVAL and REFVAL fields.
111	Invalid.

Table 6.2 - Knock KO Select Definition

6.8 Knock Registers

Address (00-13) R-KNKCOEF –Read Knock IIR Coefficient Locations		
Bit #	Data from PROSAK	Reset
15	Coefficient Sign	
14-13	Coefficient Magnitude Integer (bit 14 is 2^{1}; bit 13 is 2^{0})	
12-2	Coefficient Magnitude Fraction (bit 12 is 2^{-1}; bit 2 is 2^{-11})	
1-0	Reserved	
Address	Data Field	Reset
00	Coefficient $a_{1,A}$	X
01	Coefficient $a_{1,B}$	X
02	Coefficient $a_{1,C}$	X
03	Coefficient $a_{1,D}$	X
04	Coefficient $b_{0,A}$	X
05	Coefficient $b_{0,B}$	X
06	Coefficient $b_{0,C}$	X
07	Coefficient $b_{0,D}$	X
08	Coefficient $b_{1,A}$	X
09	Coefficient $b_{1,B}$	X
0A	Coefficient $b_{1,C}$	X
0B	Coefficient $b_{1,D}$	X
0C	Coefficient $b_{2,A}$	X
0D	Coefficient $b_{2,B}$	X
0E	Coefficient $b_{2,C}$	X
0F	Coefficient $b_{2,D}$	X
10	Coefficient $a_{2,A}$	X
11	Coefficient $a_{2,B}$	X
12	Coefficient $a_{2,C}$	X
13	Coefficient $a_{2,D}$	X

These 20 registers are the IIR knock coefficient locations. The coefficient is a fourteen bit sign-magnitude number and has a range of $-4.0 < \text{coefficient} < 4.0$.

Address (40–4B) R-KNKTHR0-11 – Read Knock Threshold Locations		
Bit #	Data from PROSAK	Reset
15-0	Threshold n	X
These 12 registers contain the knock thresholds. The threshold is a sixteen bit positive number. Address 40 contains the threshold for cylinder 0, and address 4B contains the threshold for cylinder 11.		

Address (4C) R-KNKCNU – Read Coefficient No Knock Up		
Bit #	Data from PROSAK	Reset
15-0	C_{nu} Coefficient No Knock Up	X
This register is the no knock up coefficient. The coefficient is a sixteen bit positive number and has a range of $0 \leq$ coefficient < 1.0.		

Address (4D) R-KNKCND – Read Coefficient No Knock Down		
Bit #	Data from PROSAK	Reset
15-0	C_{nd} Coefficient No Knock Down	X
This register is the no knock down coefficient. The coefficient is a sixteen bit positive number and has a range of $0 \leq$ coefficient < 1.0.		

Address (4E) R-KNKCKU – Read Coefficient Knock Up		
Bit #	Data from PROSAK	Reset
15-0	C_{ku} Coefficient Knock Up	X
This register is the knock up coefficient location. The coefficient is a sixteen bit positive number and has a range of $0 \leq$ coefficient < 1.0.		

Address (4F) R-KNKCKD – Read Coefficient Knock Down		
Bit #	Data from PROSAK	Reset
15-0	C_{kd} Coefficient Knock Down	X
This register is the knock down coefficient. The coefficient is a sixteen bit positive number and has a range of $0 \leq$ coefficient < 1.0.		

Address (50) R-REFA0H – Read Reference Average 0 High		
Bit #	Data from PROSAK	Reset
15-0	Reference Average 0 High (bits 31-16)	X
This is the upper 16 bits of the reference average 0 value. The average result is a 32 bit positive number.		

Address (51) R-REFA0L – Read Reference Average 0 Low		
Bit #	Data from PROSAK	Reset
15-0	Reference Average 0 Low (bits 15-0)	X
This is the lower 16 bits of the reference average 0 value. The average result is a 32 bit positive number.		

Address (52) R-REFA1H - Read Reference Average 1 High		
Bit #	Data from PROSAK	Reset
15-0	Reference Average 1 High (bits 31-16)	X
This is the upper 16 bits of the reference average 1 value. The average result is a 32 bit positive number.		

Address (53) R-REFA1L – Read Reference Average 1 Low		
Bit #	Data from PROSAK	Reset
15-0	Reference Average 1 Low (bits 15-0)	X
This is the lower 16 bits of the reference average 1 value. The average result is a 32 bit positive number.		

Address (54) R-KNKR – Read Knock Ratio		
Bit #	Data from PROSAK	Reset
15-0	KNOCK / REF_{avg} ratio	X
This is the KNOCK / REFavg ratio register. The ratio is a sixteen bit positive number.		

Address (55) R-KNKI – Read Knock Intensity		
Bit #	Data from PROSAK	Reset
15-0	Knock Intensity	X
This is the Knock Intensity register. The intensity is a sixteen bit positive number.		

Address (58) R-KNKIH – Read Knock Integrator High		
Bit #	Data from PROSAK	Reset
15-0	Knock Integrator High (bits 31-16)	X
This register is the upper 16 bits of the knock integrator value. The integrator result is a 32 bit positive number.		

Address (59) R-KNKIL – Read Knock Integrator Low		
Bit #	Data from PROSAK	Reset
15-0	Knock Integrator Low (bits 15-0)	X
This register is the lower 16 bits of the knock integrator value. The integrator result is a 32 bit positive number.		

Address (5A) R-REFIH – Read Reference Integrator High		
Bit #	Data from PROSAK	Reset
15-0	Reference Integrator High (bits 31-16)	X
This register is the upper 16 bits of the reference integrator value. The integrator result is a 32 bit positive number.		

Address (5B) R-REFIL – Read Reference Integrator Low		
Bit #	Data from PROSAK	Reset
15-0	Reference Integrator Low (bits 15-0)	X
This register is the lower 16 bits of the reference integrator value. The integrator result is a 32 bit positive number.		

Address (60) R-KNKSS – Read Knock Sensor Select		
Bit #	Data from PROSAK	Reset
15-12	Unused	0
11	Cylinder 11, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
10	Cylinder 10, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
9	Cylinder 9, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
8	Cylinder 8, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
7	Cylinder 7, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
6	Cylinder 6, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
5	Cylinder 5, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
4	Cylinder 4, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
3	Cylinder 3, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
2	Cylinder 2, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
1	Cylinder 1, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
0	Cylinder 0, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
This register contains the sensor select for all 12 cylinders.		

Address (76) R-KNKSETUP0 –Read Knock Setup Register		
Bit #	Data from PROSAK	Reset
15-6	Unused	0
5-0	KNKSCALE – Determines the position of the decimal point for the KNKR0-11, KNKR, and KNKI.. 1F – bbbbbbbbbbbbbbb. 20 – bbbbbbbbbbbbbb.b 21 – bbbbbbbbbbbbb.bb 22 – bbbbbbbbbbbb.bbb 23 – bbbbbbbbbbb.bbbb 24 – bbbbbbbbbb.bbbbb 25 – bbbbbbbbb.bbbbbb 26 – bbbbbbbb.bbbbbbb 27 – bbbbbbb.bbbbbbbb 28 – bbbbbb.bbbbbbbbb 29 – bbbbb.bbbbbbbbbb 2A – bbbb.bbbbbbbbbbb 2B – bbb.bbbbbbbbbbbb 2C – bb.bbbbbbbbbbbbb 2D – b.bbbbbbbbbbbbbb 2E – .bbbbbbbbbbbbbbb 2F - .bbbbbbbbbbbbbbb	27
This register is used to setup and monitor the knock block. Bits 5-0 are read-only bits, and are status bits.		

Address (77) R-KNKSETUP1 –Read Knock Setup Register		
Bit #	Data from PROSAK	Reset
15-5	Unused	0
6	SENALLUP – Sensor always update 0 – Sensor select to logic is only updated with the value in the KNKSS register after the falling window, and the window's calculation is finished. 1 – Sensor select is always updated with the value in the KNKSS register.	0
5	IIRENBLE – Enable IIR filter. 0 – IIR Filter disabled, filter coefficients can be modified. 1 – IIR Filter enabled, filter coefficients locked	0
4	KNKGAIN – A/D Gain. 0 – 1x 1 – 2x	0
3	SSCHG – Sensor Select Change. Determines when to change the sensor select, and sample the cylinder counter. 0 – After the knock calculations are complete 1 – After the reference calculations are complete	0
2-0	KOSEL – Selects the function of the KO pin 000 – 0 001 - Knock Indicator 010 - Knock Valid 100 - Reference Valid 110 - Knock Valid and Reference Valid	0
This register is used to setup and monitor the knock block.		

Address (78) R-KNKSTAT0 – Read Knock Status Register		
Bit #	Data from PROSAK	Reset
15-5	Unused	0
4	Knock Detect Divider Overflow	0
3	Knock IIR Overflow Detection Biquad D.	0
2	Knock IIR Overflow Detection Biquad C.	0
1	Knock IIR Overflow Detection Biquad B.	0
0	Knock IIR Overflow Detection Biquad A.	0
This register contains the status bits for knock including the knock IIR overflow detection bits. The Overflow bits can only be cleared by reading asserted, and writing a 0 in the desired bit position.		

Address (79) R-KNKSTAT1 – Read Knock Status Register		
Bit #	Data from PROSAK	Reset
15-7	Unused	0
6	REFVAL – Reference Calculation Valid 0 – Reference average is not valid. 1 – Reference average is valid.	0
5	KNOCKVAL – Knock Calculation Valid 0 – Knock Ratio and Intensity are not valid. 1 – Knock Ratio and Intensity are valid.	0
4	KIFLG – Knock Indicator 0 – Knock not detected. 1 – Knock detected.	0
3-0	KNKCYL – Knock Cylinder current value	0
This register contains the status bits for knock. Bits 6-0 are read-only bits.		

Address (80-93) W-KNKCOEF –Write Knock IIR Coefficient Locations		
Bit #	Data to PROSAK	Reset
31-24	Address (80-93)	0
23-16	Unused	0
15	Coefficient Sign	X
14-13	Coefficient Magnitude Integer (bit 14 is 2^1; bit 13 is 2^0)	X
12-2	Coefficient Magnitude Fraction (bit 12 is 2^{-1}; bit 2 is 2^{-11})	X
1-0	Reserved	
Address	Data Field	Reset
80	Coefficient $a_{1,A}$	X
81	Coefficient $a_{1,B}$	X
82	Coefficient $a_{1,C}$	X
83	Coefficient $a_{1,D}$	X
84	Coefficient $b_{0,A}$	X
85	Coefficient $b_{0,B}$	X
86	Coefficient $b_{0,C}$	X
87	Coefficient $b_{0,D}$	X
88	Coefficient $b_{1,A}$	X
89	Coefficient $b_{1,B}$	X
8A	Coefficient $b_{1,C}$	X
8B	Coefficient $b_{1,D}$	X
8C	Coefficient $b_{2,A}$	X
8D	Coefficient $b_{2,B}$	X
8E	Coefficient $b_{2,C}$	X
8F	Coefficient $b_{2,D}$	X
90	Coefficient $a_{2,A}$	X
91	Coefficient $a_{2,B}$	X
92	Coefficient $a_{2,C}$	X
93	Coefficient $a_{2,D}$	X
These 20 registers are the IIR knock coefficient locations. The coefficient is a fourteen bit sign-magnitude number and has a range of -4.0 < coefficient < 4.0.		

Address (C0–CB) W-KNKTHR0-11 – Write Knock Threshold Locations		
Bit #	Data to PROSAK	Reset
31-24	Address (C0-CB)	0
23-16	Unused	0
15-0	Threshold n	X
These 12 registers contain the knock thresholds. The threshold is a sixteen bit positive number. Address C0 contains the threshold for cylinder 0, and address CB contains the threshold for cylinder 11.		

Address (CC) W-KNKCNU – Write Coefficient No Knock Up		
Bit #	Data to PROSAK	Reset
31-24	Address (CC)	0
23-16	Unused	0
15-0	C_{nu} Coefficient No Knock Up	X
This register is the no knock up coefficient. The coefficient is a sixteen bit positive number and has a range of $0 \leq$ coefficient < 1.0.		

Address (CD) W-KNKCND – Write Coefficient No Knock Down		
Bit #	Data to PROSAK	Reset
31-24	Address (CD)	0
23-16	Unused	0
15-0	C_{nd} Coefficient No Knock Down	X
This register is the no knock down coefficient. The coefficient is a sixteen bit positive number and has a range of $0 \leq$ coefficient < 1.0.		

Address (CE) W-KNKCKU – Write Coefficient Knock Up		
Bit #	Data to PROSAK	Reset
31-24	Address (CE)	0
23-16	Unused	0
15-0	C_{ku} Coefficient Knock Up	X
This register is the knock up coefficient location. The coefficient is a sixteen bit positive number and has a range of $0 \leq$ coefficient < 1.0.		

Address (CF) W-KNKCKD – Write Coefficient Knock Down		
Bit #	Data to PROSAK	Reset
31-24	Address (CF)	0
23-16	Unused	0
15-0	C_{kd} Coefficient Knock Down	X
This register is the knock down coefficient. The coefficient is a sixteen bit positive number and has a range of $0 \leq$ coefficient < 1.0.		

Address (D0) W-REFA0H – Write Reference Average 0 High		
Bit #	Data to PROSAK	Reset
31-24	Address (D0)	0
23-16	Unused	0
15-0	Reference Average 0 High (bits 31-16)	X
This is the upper 16 bits of the reference average 0 value. The average result is a 32 bit positive number.		

Address (D1) W-REFA0L – Write Reference Average 0 Low		
Bit #	Data to PROSAK	Reset
31-24	Address (D1)	0
23-16	Unused	0
15-0	Reference Average 0 Low (bits 15-0)	X
This is the lower 16 bits of the reference average 0 value. The average result is a 32 bit positive number.		

Address (D2) W-REFA1H - Write Reference Average 1 High		
Bit #	Data to PROSAK	Reset
31-24	Address (D2)	0
23-16	Unused	0
15-0	Reference Average 1 High (bits 31-16)	X
This is the upper 16 bits of the reference average 1 value. The average result is a 32 bit positive number.		

Address (D3) W-REFA1L – Write Reference Average 1 Low		
Bit #	Data to PROSAK	Reset
31-24	Address (D3)	0
23-16	Unused	0
15-0	Reference Average 1 Low (bits 15-0)	X
This is the lower 16 bits of the reference average 1 value. The average result is a 32 bit positive number.		

Address (D4) W-KNKR – Write Knock Ratio		
Bit #	Data to PROSAK	Reset
31-24	Address (D4)	0
23-16	Unused	0
15-0	KNOCK / REF_{avg} ratio	X
This is the KNOCK / REFavg ratio register. The ratio is a sixteen bit positive number.		

Address (D5) W-KNKI – Write Knock Intensity		
Bit #	Data to PROSAK	Reset
31-24	Address (D5)	0
23-16	Unused	0
15-0	Knock Intensity	X
This is the Knock Intensity register. The intensity is a sixteen bit positive number.		

Address (D8) W-KNKIH – Write Knock Integrator High		
Bit #	Data to PROSAK	Reset
31-24	Address (D8)	0
23-16	Unused	0
15-0	Knock Integrator High (bits 31-16)	X
This register is the upper 16 bits of the knock integrator value. The integrator result is a 32 bit positive number. This register can only be accessed when the integrator is not integrating (when WINK is low).		

Address (D9) W-KNKIL – Write Knock Integrator Low		
Bit #	Data to PROSAK	Reset
31-24	Address (D9)	0
23-16	Unused	0
15-0	Knock Integrator Low (bits 15-0)	X
This register is the lower 16 bits of the knock integrator value. The integrator result is a 32 bit positive number. This register can only be accessed when the integrator is not integrating (when WINK is low).		

Address (DA) W-REFIH – Write Reference Integrator High		
Bit #	Data to PROSAK	Reset
31-24	Address (DA)	0
23-16	Unused	0
15-0	Reference Integrator High (bits 31-16)	X
This register is the upper 16 bits of the reference integrator value. The integrator result is a 32 bit positive number. This register can only be accessed when the integrator is not integrating (when WINR is low).		

Address (E0) W-KNKSS – Write Knock Sensor Select		
Bit #	Data to PROSAK	Reset
31-24	Address (E0)	0
23-12	Unused	0
11	Cylinder 11, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
10	Cylinder 10, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
9	Cylinder 9, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
8	Cylinder 8, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
7	Cylinder 7, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
6	Cylinder 6, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
5	Cylinder 5, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
4	Cylinder 4, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
3	Cylinder 3, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
2	Cylinder 2, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
1	Cylinder 1, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
0	Cylinder 0, 0 – Knock Sensor 0, 1 – Knock Sensor 1	0
This register contains the sensor select for all 12 cylinders.		

Address (F6) W-KNKSETUP0 –Write Knock Setup Register		
Bit #	Data to PROSAK	Reset
15-8	Address (F6)	0
7-6	Unused	0
5-0	KNKSCALE – Determines the position of the decimal point for the KNKR0-11, KNKR, and KNKI.. 1F – bbbbbbbbbbbbbbb. 20 – bbbbbbbbbbbbbbb.b 21 – bbbbbbbbbbbbbb.bb 22 – bbbbbbbbbbbbb.bbb 23 – bbbbbbbbbbbb.bbbb 24 – bbbbbbbbbbb.bbbbb 25 – bbbbbbbbbb.bbbbbb 26 – bbbbbbbbb.bbbbbbb 27 – bbbbbbbb.bbbbbbbb 28 – bbbbbbb.bbbbbbbbb 29 – bbbbbb.bbbbbbbbbb 2A – bbbbb.bbbbbbbbbbb 2B – bbbb.bbbbbbbbbbbb 2C – bbb.bbbbbbbbbbbbb 2D – bb.bbbbbbbbbbbbbb 2E – b.bbbbbbbbbbbbbbb 2F - .bbbbbbbbbbbbbbbb	27
This register is used to setup and monitor the knock block.		

Address (F7) W-KNKSETUP1 –Write Knock Setup Register		
Bit #	Data to PROSAK	Reset
15-8	Address (F7)	0
7	Unused	0
6	SENALLUP – Sensor always update 0 – Sensor select to logic is only updated with the value in the KNKSS register after the falling window, and the window's calculation is finished. 1 – Sensor select is always updated with the value in the KNKSS register.	0
5	IIRENABLE – Enable IIR Filter. 0 – IIR Filter disabled, filter coefficients can be modified. 1 – IIR Filter enabled, filter coefficients locked	0
4	KNKGAIN – A/D Gain. 0 – 1x 1 – 2x	0
3	SSCHG – Sensor Select Change. Determines when to change the sensor select, and sample the cylinder counter. 0 – After the knock calculations are complete 1 – After the reference calculations are complete	0
2-0	KOSEL – Selects the function of the KO pin 000 – 0 001 - Knock Indicator 010 - Knock Valid 100 - Reference Valid 110 - Knock Valid and Reference Valid	0
This register is used to setup and monitor the knock block. Bits 4-0 are writeable.		

Address (F8) W-KNKSTAT0 – Write Knock Status Register		
Bit #	Data to PROSAK	Reset
15-8	Address (F8)	0
7-5	Unused	0
4	Knock Detect Divider Overflow	0
3	Knock IIR Overflow Detection Biquad D.	0
2	Knock IIR Overflow Detection Biquad C.	0
1	Knock IIR Overflow Detection Biquad B.	0
0	Knock IIR Overflow Detection Biquad A.	0
This register contains the status bits for knock including the knock IIR overflow detection bits. The Overflow bits can only be cleared by reading asserted value, and writing a 0 in the desired bit position.		

7. Calibration Data Port

The Calibration port is a serial port that brings out essential internal states from the Knock Processing. This will allow the Calibrator the ability to see what is going on inside the PROSAK IC. The Calibration port output will be sent to an external calibration device that will allow the calibrator to monitor all the data flowing through the Knock.

The Calibration data will be transmitted out the CO pin as packets of data where the packet length is either 88 or 56 bits. The data will be transmitted most significant bit first using Manchester encoding at a data rate of CLK/2. Figure 7.1 describes the encoding. Between data packets the CO pin will be held low.

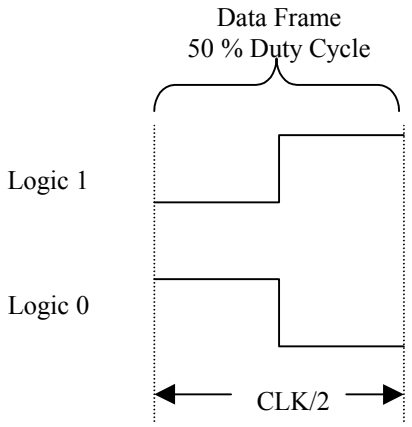


Figure 7.1 - Calibration Output Waveform

The CALSETUP register controls the setup of the calibration port. The CalSel field determines if the calibration port is enabled, and what data is to be transmitted. If CalSel is zero, then the CO pin will always be low. If CalSel is non-zero, then the calibration port is enabled, and CO will output the Manchester data when available. In order to synchronize the receiver on the external calibration device, the first 8 data frames of any packet will be hex AA. The CalSel Field also selects which circuit will be outputted on the calibration port. Table 7.1 defines the CalSel Field encoding.

CalSel	Description
0	Calibration port disabled, CO pin will output logic 0
1	Select Backend Calibration as output for CO
2	Select IIR+COMB Calibration as output for CO
3	Select IIR+COEF Calibration as output for CO

Table 7.1 - CalSel Field Definition

7.1 Implementation of the Calibration Data Port

7.1.1 Backend Calibration Output

If the CalSel field is one, then the Backend Processing data will be sent out the calibration port. The backend circuit will transmit data packets when the corresponding window is finished, and the backend calculations are complete. The data packets consist of a sync word of AA, followed by a four-bit header that defines the data type, and the length of the data packet, followed by the data. Table 7.2 defines the two types of backend packets.

Packet Name	Number of Bits
Knock Backend Packet	88
Reference Backend Packet	88

Table 7.2 - Backend Packet Types

7.1.1.1 Knock Backend Packet

The Knock Backend Packet will be used to monitor the knock backend processing. The Knock Backend Packet consists of the knock integration result, the knock vs. average ratio, the current threshold value, the current cylinder value, the knock scale value, and the knock indication value. Table 7.3 shows the bit order of the knock backend packet.

Bit Number	Description
87-80	Sync word of AA
79-76	Header word of 1
75-44	32 bit Unsigned Knock Integration
43-28	16 bit Unsigned Knock Ratio
27-12	16 bit Unsigned Knock Threshold
11	Knock Indication Flag
10	Divide Overflow
9-6	4 bit Knock Cylinder
5-0	6 bit knock scale value

Table 7.3 - Knock Backend Packet Definition

7.1.1.2 Reference Backend Packet

The Reference Backend Packet will be used to monitor the reference backend processing. The Reference Backend Packet consists of the reference integration result, the new reference average, the current sensor select value, the current cylinder value, and the knock scale value. Table 7.4 shows the bit ordering of the reference backend packet.

Bit Number	Description
87-80	Sync word of AA
79-76	Header word of 5
75-44	32 bit Unsigned Reference Integration
43-12	32 bit Unsigned Reference Average
11	Sensor select
10	Unused (zero padding)
9-6	4 bit Knock Cylinder
5-0	6 bit knock scale value

Table 7.4 - Reference Backend Packet Definition

7.1.2 IIR+COMB Calibration Output

If the CalSel field is two, then the IIR+COMB Processing data will be sent out the calibration port. The IIR+COMB calibration has only one type of packet. The packet will be sent out at the data rate of MODCLK/32. Table 7.5 defines the one type of IIR+COMB packet.

Packet Name	Number of Bits
IIR+COMB Packet	56

Table 7.5 - IIR+COMB Packet Type

7.1.2.1 IIR+COMB Packet

The IIR+COMB Packet will be used to monitor the IIR and COMB filter processing. The IIR+COMB Packet consists of the COMB filter result, the IIR filter result, the IIR filter overflow bits, and the sampled knock and reference window values. Table 7.6 shows the bit order of the IIR+COMB packet.

Bit Number	Description
55-48	Sync word of AA
47-44	Header word of 2
43-25	19 bit Signed IIR Result
24	Sampled Knock Window
23	Sampled Reference Window
22	IIR Overflow for Biquad D
21	IIR Overflow for Biquad C
20	IIR Overflow for Biquad B
19	IIR Overflow for Biquad A
18-2	17 bit Signed COMB Result
1-0	Unused (zero padding)

Table 7.6 - IIR+COMB Packet Definition

7.1.3 IIR+COEF Calibration Output

If the CalSel field is three, then the IIR+COEF Processing data will be sent out the calibration port. The IIR+COEF calibration has only one type of packet. The packet will be sent out at the data rate of MODCLK/32. Table 7.7 defines the one type of IIR+COEF packet.

Packet Name	Number of Bits
IIR+COEF Packet	56

Table 7.7 - IIR+COEF Packet Type

7.1.3.1 IIR+COEF Packet

The IIR+COEF Packet will be used to monitor just the IIR filter processing. The IIR+COEF Packet consists of the IIR filter result, the IIR filter overflow bits, the sampled knock and reference window values, and one of the IIR filter coefficients, along with an IIR filter coefficient address. After a IIR+COEF packet has been transmitted, the IIR filter coefficient address will be incremented such that after 20 packets, all the filter coefficients will have been transmitted. Table 7.8 shows the bit order of the IIR+COEF packet. Table 7.9 shows the order that the IIR filter coefficients are output.

Bit Number	Description
55-48	Sync word of AA
47-44	Header word of 3
43-25	19 bit Signed IIR Result
24	Sampled Knock Window
23	Sampled Reference Window
22	IIR Overflow for Biquad D
21	IIR Overflow for Biquad C
20	IIR Overflow for Biquad B
19	IIR Overflow for Biquad A
18-5	14 bit Signed IIR Filter Coefficient
4-0	5 bit IIR Coefficient address

Table 7.8 - IIR+COEF Packet Definition

Packet Number	Coefficient
0	Coefficient $a_{1,A}$
1	Coefficient $a_{1,B}$
2	Coefficient $a_{1,C}$
3	Coefficient $a_{1,D}$
4	Coefficient $b_{0,A}$
5	Coefficient $b_{0,B}$
6	Coefficient $b_{0,C}$
7	Coefficient $b_{0,D}$
8	Coefficient $b_{1,A}$
9	Coefficient $b_{1,B}$
10	Coefficient $b_{1,C}$
11	Coefficient $b_{1,D}$
12	Coefficient $b_{2,A}$
13	Coefficient $b_{2,B}$
14	Coefficient $b_{2,C}$
15	Coefficient $b_{2,D}$
16	Coefficient $a_{2,A}$
17	Coefficient $a_{2,B}$
18	Coefficient $a_{2,C}$
19	Coefficient $a_{2,D}$

Table 7.9 - IIR+COEF Packet Coefficient Order

7.2 Calibration Registers

Address (75) R-CALSETUP –Read Calibration Setup Register		
Bit #	Data from PROSAK	Reset
15-2	Unused	0
1-0	CALSEL – These two bits select which circuit to calibrate. 00 – Calibration Disabled 01 – Backend Calibration. 10 – IIR+COMB Calibration. 11 – IIR+COEF Calibration.	0
This register controls the setup and operation of the calibration port.		

Address (F5) W-CALSETUP –Write Calibration Setup Register		
Bit #	Data to PROSAK	Reset
15-8	Address (F5)	0
7-2	Unused	0
1-0	CALSEL – These two bits select which circuit to calibrate. 00 – Calibration Disabled 01 – Backend Calibration. 10 – IIR+COMB Calibration. 11 – IIR+COEF Calibration.	0
This register controls the setup and operation of the calibration port.		

Appendix A – Calibration Tool

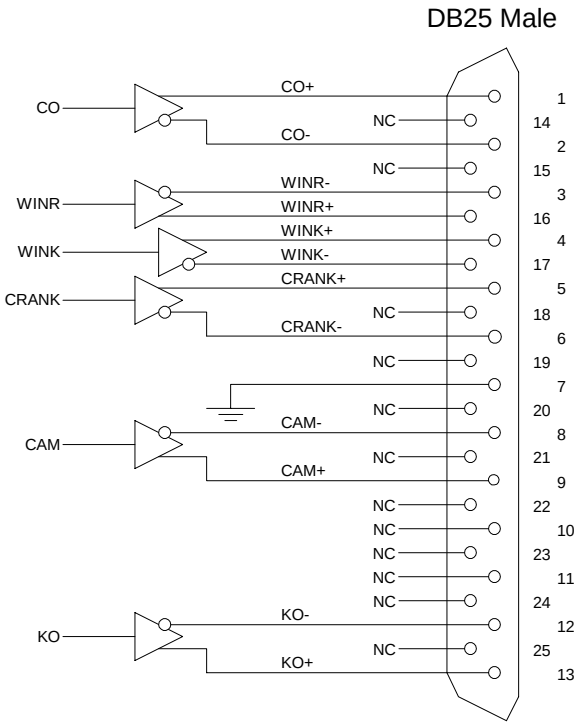


Figure A.1 – Example of Calibration Tool Connector

* Note:

1. The CRANK and CAM signals are sent to the calibration tool to determine engine position. Alternate methods such as an encoder may be used.
2. The CO, KO, WINK signals are required for a single-window system.
3. The CO, KO, WINK, and WINR signals are required for a dual-window system.

8. Version Log

Version	Date	Author	Revision Notes
1.0	06/25/01	SJR	Initial document for single-window application (no reference window). This version was taken from the target design specification.
1.1	07/19/01	SJR	Added - Recommended input circuit - Example interface circuit and connector for knock tool.
1.2	09/06/01	SJR	Added - Functionality description for two-window system (reference window plus knock window). - Software procedures for IC initialization, synchronization, and normal operation.
1.3	09/13/01	SJR	Changed - Figure 4: VDDD and VSSD pins reversed. Removed - Removed reference to SPI operation modes of "Normal" and "out of RESET".
1.4	09/26/01	SJR	Added - Calibration Output (CO) pin description and functionality. Changed - Renumbered figures and tables to match section numbers.